pattern, wherein a thickness of an edge portion of the second resist pattern is smaller than a thickness of a middle portion of the second resist pattern;

forming a rectangular first gate electrode over the first semiconductor by dry etching using the first resist pattern;

forming a second gate electrode by dry etching using the second resist pattern over the second semiconductor, wherein a thickness of an edge portion of the second gate electrode is smaller than a thickness of a middle portion of the second gate electrode;

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introducing an impurity element into the first semiconductor with the first gate electrode as a mask to form a first impurity region in the first semiconductor, wherein the first impurity region is not overlapped with the first gate electrode; and

introducing the impurity element into the second semiconductor with the second gate electrode as a mask to form a second impurity region and a third impurity region in the second semiconductor, wherein the second impurity region is not overlapped with the second gate electrode and the third impurity region is overlapped with the edge portion of the second gate electrode.

3. A method of manufacturing a semiconductor device, the method comprising:

forming a conductive film over a first semiconductor and a second semiconductor with an insulating film therebetween;

forming a rectangular first resist pattern on the conductive film over the first semiconductor;

forming a second resist pattern on the conductive film over the second semiconductor by using a photomask having a diffraction grating pattern or a reticle having a diffraction grating pattern, wherein a thickness of an edge portion of the second resist pattern is smaller than a thickness of a middle portion of the second resist pattern;

forming a rectangular first gate electrode over the first semiconductor by dry etching using the first resist pattern;

forming a second gate electrode by dry etching using the second resist pattern over the second semiconductor, wherein a thickness of an edge portion of the second gate electrode is smaller than a thickness of a middle portion of the second gate electrode;

introducing an impurity element into the first semiconductor with the first gate electrode as a mask to form a first impurity region in the first semiconductor, wherein the first impurity region is not overlapped with the first gate electrode;

introducing the impurity element into the second semiconductor with the second gate electrode as a mask to form a second impurity region in the second semiconductor, wherein the second impurity region is not overlapped with the second gate electrode;

removing the first and the second resist patterns;

forming a third resist pattern covering the first gate electrode;

introducing the impurity element into the first semiconductor with the third resist pattern as a mask to form a third impurity region in the first semiconductor, wherein the third impurity region is not overlapped with the third resist pattern and the first gate electrode; and

introducing the impurity element into the second semiconductor with the second gate electrode as a mask to form a fourth impurity region and a fifth impurity region in the second semiconductor, wherein the fourth impurity region is not overlapped with the second gate electrode and the fifth impurity region is overlapped with the edge portion of the second gate electrode.

4. A method of manufacturing a semiconductor device, the method comprising:

forming a conductive film over a semiconductor with an insulating film therebetween;

forming a resist pattern on the conductive film by using a photomask having a translucent film portion or a reticle having a translucent film portion, wherein a thickness of an edge portion of the resist pattern is smaller than a thickness of a middle portion of the resist pattern;

forming a gate electrode by etching using the resist pattern, wherein a thickness of an edge portion of the gate electrode is smaller than a thickness of a middle portion of the gate electrode; and

introducing an impurity element into the semiconductor with the gate electrode as a mask to form a first impurity region and a second impurity region in the semiconductor, wherein the first impurity region is not overlapped with the gate electrode and the second impurity region is overlapped with the edge portion of the gate electrode.

5. A method of manufacturing a semiconductor device, the method comprising:

forming a conductive film over a first semiconductor and a second semiconductor with an insulating film therebetween;

forming a rectangular first resist pattern on the conductive film over the first semiconductor;

forming a second resist pattern on the conductive film over the second semiconductor by using a photomask having a translucent film portion or a reticle having a translucent film portion, wherein a thickness of an edge portion of the second resist pattern is smaller than a thickness of a middle portion of the second resist pattern;

forming a rectangular first gate electrode over the first semiconductor by dry etching using the first resist pattern;

forming a second gate electrode by dry etching using the second resist pattern over the second semiconductor, wherein a thickness of an edge portion of the second gate electrode is smaller than a thickness of a middle portion of the second gate electrode;

introducing an impurity element into the first semiconductor with the first gate electrode as a mask to form a first impurity region in the first semiconductor, wherein the first impurity region is not overlapped with the first gate electrode; and

introducing the impurity element into the second semiconductor with the second gate electrode as a mask to form a second impurity region and a third impurity region in the second semiconductor, wherein the second impurity region is not overlapped with the second gate electrode and the third impurity region is overlapped with the edge portion of the second gate electrode.

6. A method of manufacturing a semiconductor device, the method comprising:

forming a conductive film over a first semiconductor and a second semiconductor with an insulating film therebetween;

forming a rectangular first resist pattern on the conductive film over the first semiconductor;

forming a second resist pattern on the conductive film over the second semiconductor by using a photomask having a translucent film portion or a reticle having a translucent film portion,

wherein a thickness of an edge portion of the second resist pattern is smaller than a thickness of a middle portion of the second resist pattern;

forming a rectangular first gate electrode over the first semiconductor by dry etching using the first resist pattern;

forming a second gate electrode by dry etching using the second resist pattern over the second semiconductor, wherein a thickness of an edge portion of the second gate electrode is smaller than a thickness of a middle portion of the second gate electrode;

introducing an impurity element into the first semiconductor with the first gate electrode as a mask to form a first impurity region in the first semiconductor, wherein the first impurity region is not overlapped with the first gate electrode;

introducing the impurity element into the second semiconductor with the second gate electrode as a mask to form a second impurity region in the second semiconductor, wherein the second impurity region is not overlapped with the second gate electrode;

removing the first and the second resist patterns;

forming a third resist pattern covering the first gate electrode;

introducing the impurity element into the first semiconductor with the third resist pattern as a mask to form a third impurity region in the first semiconductor, wherein the third impurity region is not overlapped with the third resist pattern and the first gate electrode;

introducing the impurity element into the second semiconductor with the second gate electrode as a mask to form a fourth impurity region and a fifth impurity region in the second semiconductor, wherein the fourth impurity region is not overlapped with the second gate electrode and the fifth impurity region is overlapped with the edge portion of the second gate electrode.

8. A method of manufacturing a semiconductor device, the method comprising:

forming a conductive film over a first semiconductor and a second semiconductor with an insulating film therebetween;

forming a rectangular first resist pattern on the conductive film over the first semiconductor;

forming a second resist pattern on the conductive film over the second semiconductor, wherein a thickness of an edge portion of the resist pattern is smaller than thickness of a middle portion of the resist pattern;

forming a rectangular first gate electrode over the first semiconductor by a first dry etching using the first resist pattern;

forming a second gate electrode by the first dry etching using the second resist pattern over the second semiconductor, wherein a thickness of an edge portion of the second gate electrode is smaller than a thickness of a middle portion of the second gate electrode;

introducing an impurity element into the first semiconductor with the first gate electrode as a mask to form a first impurity region in the first semiconductor, wherein the first impurity region is not overlapped with the first gate electrode;

introducing an impurity element into the second semiconductor with the second gate electrode as a mask to form a second impurity region and a third impurity region in the second semiconductor, wherein the second impurity region is not overlapped with the second gate electrode and the third impurity region is overlapped with the edge portion of the second gate electrode; and

making the edge portion of the second gate electrode recede by a second dry etching.

9. A method of manufacturing a semiconductor device, the method comprising:

forming a conductive film over a first semiconductor and a second semiconductor with an insulating film therebetween;

forming a first resist pattern on the conductive film over the first semiconductor and a second resist pattern on the conductive film over the second semiconductor, wherein a thickness of an edge portion of the first resist pattern and a second thickness of an edge portion of the second resist pattern are smaller than thickness of a middle portion each of the first and the second resist patterns;

forming a first gate electrode by a first dry etching using the first resist pattern, wherein the first thickness of an edge portion of the first gate electrode is smaller than a thickness of a middle portion of the first gate electrode, forming the second gate electrode by the first dry

etching using the second resist pattern, wherein the second thickness of an edge portion of the second gate electrode is smaller than a thickness of a middle portion of the second gate electrode;

removing the first and the second resist patterns;

introducing an impurity element into the first semiconductor with the first gate electrode as a mask to form a first impurity region and a second impurity region in the first semiconductor, wherein the first impurity region is not overlapped with the first gate electrode and the second impurity region is overlapped with the edge portion of the first gate electrode;

introducing the impurity element into the second semiconductor with the second gate electrode as a mask to form a third impurity region and a fourth impurity region in the second semiconductor, wherein the third impurity region is not overlapped with the second gate electrode and the fourth impurity region is overlapped with the edge portion of the second gate electrode;

making the edge portions of the first and the second gate electrodes recede by a second dry etching;

forming a third resist pattern over the first gate electrode, wherein the second gate electrode is exposed from the third resist pattern; and

making the edge portion of the second gate electrode recede by a third dry etching.

10. A method of manufacturing a semiconductor device, the method comprising:

forming a conductive film over a semiconductor with an insulating film therebetween;

forming a rectangular first resist pattern on the conductive film;

forming a second resist pattern on the conductive film, wherein a thickness of an edge portion of the second resist pattern is smaller than thickness of a middle portion of the second resist pattern;

forming a rectangular first gate electrode by a first dry etching using the first resist pattern;

forming a second gate electrode by the first dry etching using the second resist pattern, wherein a thickness of an edge portion of the second gate electrode is smaller than a thickness of a middle portion of the second gate electrode;

removing the first and the second resist patterns;

introducing an impurity element into the semiconductor with the first gate electrode as a mask to form a first impurity region in the semiconductor, wherein the first impurity region is not overlapped with the first gate electrode;

introducing the impurity element into the semiconductor with the second gate electrode as a mask to form a second impurity region and a third impurity region in the semiconductor, wherein the second impurity region is not overlapped with the second gate electrode and the third impurity region is overlapped with the edge portion of the second gate electrode; and

making the edge portion of the second gate electrode recede by a second dry etching.

18. The method of manufacturing a semiconductor device according to claim 1, wherein the edge portion of the resist pattern has a tapered configuration.

19. The method of manufacturing a semiconductor device according to claim 2, wherein the edge portion of the resist pattern has a tapered configuration.

20. The method of manufacturing a semiconductor device according to claim 3, wherein the edge portion of the resist pattern has a tapered configuration.

21. The method of manufacturing a semiconductor device according to claim 4, wherein the edge portion of the resist pattern has a tapered configuration.

22. The method of manufacturing a semiconductor device according to claim 5, wherein the edge portion of the resist pattern has a tapered configuration.

23. The method of manufacturing a semiconductor device according to claim 6, wherein the edge portion of the resist pattern has a tapered configuration.

24. The method of manufacturing a semiconductor device according to claim 7, wherein the edge portion of the resist pattern has a tapered configuration.

25. The method of manufacturing a semiconductor device according to claim 8, wherein the edge portion of the resist pattern has a tapered configuration.

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26. The method of manufacturing a semiconductor device according to claim 9, wherein the edge portion of the resist pattern has a tapered configuration.

27. The method of manufacturing a semiconductor device according to claim 10, wherein the edge portion of the resist pattern has a tapered configuration.